```
OrCAD PLD COMPILER  V4.02   2/7/91  (Source file .\MIB2_G0.PLD)

  1  This file contains the logic necessary for a GAL16V8 to perform I/O
  2  Decoding for the Micro Innovations Multipurpose Interface board (MIB2).
  3  Another version of this GAL will be used for the PMIF board (with the
  4  disk interface logic).
  5
  6  Address map:
  7
  8  Printer Data out                    40H
  9  Printer Status in                   40H
 10  Memory Board Bank Switching Port    42H
 11
 12  I/O Pin Definitions:
 13
 14  |GAL16V8   1:A7,           2:A3,           3:RD,           4:WR,
 15  |          5:A6,           6:A5,           7:A4,           8:A0,
 16  |          9:A1,           11:IORQ,        12:SIOEN,       13:A2,
 17  |          14:MEBS,        18:PDATA,       19:PSTAT
 18
 19  Acronyms:
 20
 21     Inputs -
 22
 23     A0-A7   = Z80 Address Lines A0 - A7
 24     WR      = Z80 Write Pulse
 25     RD      = Z80 Read Pulse
 26     IORQ    = Z80 I/O Request Pulse
 27
 28     Outputs:
 29
 30     MEBS    = Memory Expansion Board Strobe
 31     SIOEN   = Serial I/O Port Enable
 32     PDATA   = Printer Output Data
 33     PSTAT   = Printer Status Register
 34
 35  |  High: A[0..7]
 36  |
 37  |  PSTAT   = (IORQ & RD & A[7..0]==40H)
 38  |  PDATA   =  IORQ & WR & A[7..0]==40H
 39  |  MEBS    =  IORQ & WR & A[7..0]==42H
 40  |  SIOEN   =  IORQ & A[7..4]==0001B
 41  |
 42  |
 43  |  Signature: "MIB2rev0"
I289  Complex GAL architecture selected.


♀RESOLVED EXPRESSIONS (Reduction 2)

Signal name      Row   Terms

PSTAT              1   A7' A3' RD  A6  A5' A4' A0' A1' IORQ  A2'

PDATA              9   A7' A3' WR  A6  A5' A4' A0' A1' IORQ  A2'

MEBS              41   A7' A3' WR  A6  A5' A4' A0' A1  IORQ  A2'

SIOEN             57   A7' A6' A5' A4  IORQ
```

SIGNAL ASSIGNMENT

| Pin | Signal name | Column | Rows Beg | Rows Avail | Rows Used | Activity | |
|---|---|---|---|---|---|---|---|
| 1. | A7 | 2 | - | - | - | High | (Clock) |
| 2. | A3 | 0 | - | - | - | High | |
| 3. | RD | 5 | - | - | - | Low | |
| 4. | WR | 9 | - | - | - | Low | |
| 5. | A6 | 12 | - | - | - | High | |
| 6. | A5 | 16 | - | - | - | High | |
| 7. | A4 | 20 | - | - | - | High | |
| 8. | A0 | 24 | - | - | - | High | |
| 9. | A1 | 28 | - | - | - | High | |
| 11. | IORQ | 31 | - | - | - | Low | (Enable) |
| 12. | SIOEN | 1 | 56 | 8 | 1 | Low | (Three-state) |
| 13. | A2 | 26 | 48 | 8 | 0 | High | (Three-state) |
| 14. | MEBS | 23 | 40 | 8 | 1 | Low | (Three-state) |
| 15. | - | 18 | 32 | 8 | 0 | | (Three-state) |
| 16. | - | 14 | 24 | 8 | 0 | | (Three-state) |
| 17. | - | 10 | 16 | 8 | 0 | | (Three-state) |
| 18. | PDATA | 7 | 8 | 8 | 1 | Low | (Three-state) |
| 19. | PSTAT | 1 | 0 | 8 | 1 | Low | (Three-state) |
| | | | | 64 | 4 (6%) | | |

I200  No fatal errors found in source code.
I201  No warnings.

♀OrCAD PLD
Type:       GAL16V8
*
QP20* QF2194* QV1024*
F0*
L0000 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0032 10 10 10 11 11 11 01 11 10 11 10 11 10 10 10 10 *
L0256 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0288 10 10 11 11 10 11 01 11 10 11 10 11 10 10 10 10 *
L1280 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L1312 10 10 11 11 10 11 01 11 10 11 10 11 10 10 01 10 *
L1792 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L1824 11 10 11 11 11 11 10 11 10 11 01 11 11 11 11 10 *
L2048 00 11 10 10 01 00 11 01 01 00 10 01 01 00 00 10 *
L2080 00 11 00 10 01 11 00 10 01 10 01 01 01 11 01 10 *
L2112 00 11 00 00 11 11 11 11 11 11 11 11 11 11 11 11 *
L2144 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L2176 11 11 11 11 11 11 11 11 11 *
C28F6*

I202  1/25/92  3:31 pm  (Saturday)
I203  Memory utilization 2057/21862 (9%)
I204  Elapsed time 7 seconds

♀